CLAIMS

1. A process for the fabrication of electronic chips from a semiconductor wafer (10) comprising, on its front face, a thin active layer (12) of semiconductor material, this process comprising the formation of etched layers on the active layer, the bonding of the wafer by its front face onto a support substrate (40), the thinning down of the semiconductor wafer via its backside, then the deposition and the etching of layers of material on its backside thus thinned, the process being characterized in that narrow vertical trenches (20, 22, 24, 26) are etched into the wafer by its front face, before the bonding operation, these trenches extending into the wafer over a depth approximately equal to the residual semiconductor wafer thickness that will remain after the thinning operation, the trenches being filled with a conducting material isolated from the active layer and forming conducting vias (20', 22', 24', 26') between the front face and the backside of the thinned layer.

2. The process as claimed in claim 1, characterized in that the trenches are formed before other deposition and etching steps of electrically functional layers on the front face of the semiconductor wafer.

3. The process as claimed in one of claims 1 and 2, characterized in that at least one trench takes the form of an alignment marker visible from the backside after thinning in order to allow alignment of the patterns for etching of the layers on the backside with respect to the patterns for etching of layers on the front face.

4. The process as claimed in one of claims 1 to 3, characterized in that at least one metal layer (44) is deposited onto the backside of the wafer after

thinning, this layer being connected, by conducting vias formed within at least one narrow trench, to at least one conducting layer (32) formed, prior to bonding the wafer onto the support substrate, on the front face of the wafer.

5. The process as claimed in claim 4, characterized in that the metal layer is a photo-masking layer designed to prevent light impinging on photosensitive parts within an image sensor formed on the wafer.

6. The process as claimed in one of claims 1 to 5, characterized in that layers of color filters are deposited onto the backside of the wafer after bonding and thinning.

7. The process as claimed in claim 6, characterized in that, after deposition of the color filters, the semiconductor wafer and its support substrate are bonded onto another, transparent, substrate (60) and the support substrate is eliminated.

8. The process as claimed in one of the preceding claims, characterized in that the trenches have their internal walls coated with thin silicon oxide (28) and are filled with polycrystalline silicon (30) that is highly doped so as to be conducting.

9. The process according to one of claims 1 to 8, characterized in that the role of at least one trench is to isolate laterally one portion of active layer from other portions of active layer, and notably to isolate a region of active layer situated underneath an external connection pad from the neighboring regions of active layer.

10. The process as claimed in one of claims 1 to 9, characterized in that the semiconductor wafer comprises

a highly-doped silicon substrate coated with a more lightly doped epitaxial layer forming the active layer, of around 5 to 20 microns thickness, and in that the depth of the trenches is substantially equal to the thickness of the epitaxial layer.

11. A color image sensor comprising

- a support substrate (40, 60),
- a thin silicon layer in which a matrix of photosensitive regions is formed,
- etched layers on a front face of this silicon layer,
- at least one metal layer and layers of color filters etched onto the other face, i.e. the backside, of the silicon layer,
- narrow vertical trenches traversing the whole of the silicon layer, having their sidewalls coated with an insulating layer and that are filled with a conducting material.

12. The color image sensor as claimed in claim 11, characterized in that at least one trench filled with conducting material forms a conducting via in contact at one side with the metal layer on the backside, and at the other with at least one conducting layer on the front face.

13. The color image sensor as claimed in claim 12, characterized in that it comprises a series of parallel vertical trenches disposed under the same contact pad for the external connection of the image sensor and electrically connected to this pad.

14. The color image sensor as claimed in one of claims 11 to 13, characterized in that at least one vertical trench forms an isolation trench between two neighboring silicon regions of the silicon layer.

15. The color image sensor as claimed in claim 14,

characterized in that the trench that forms an isolation trench completely surrounds a silicon region situated underneath a contact pad for the external connection of the image sensor.